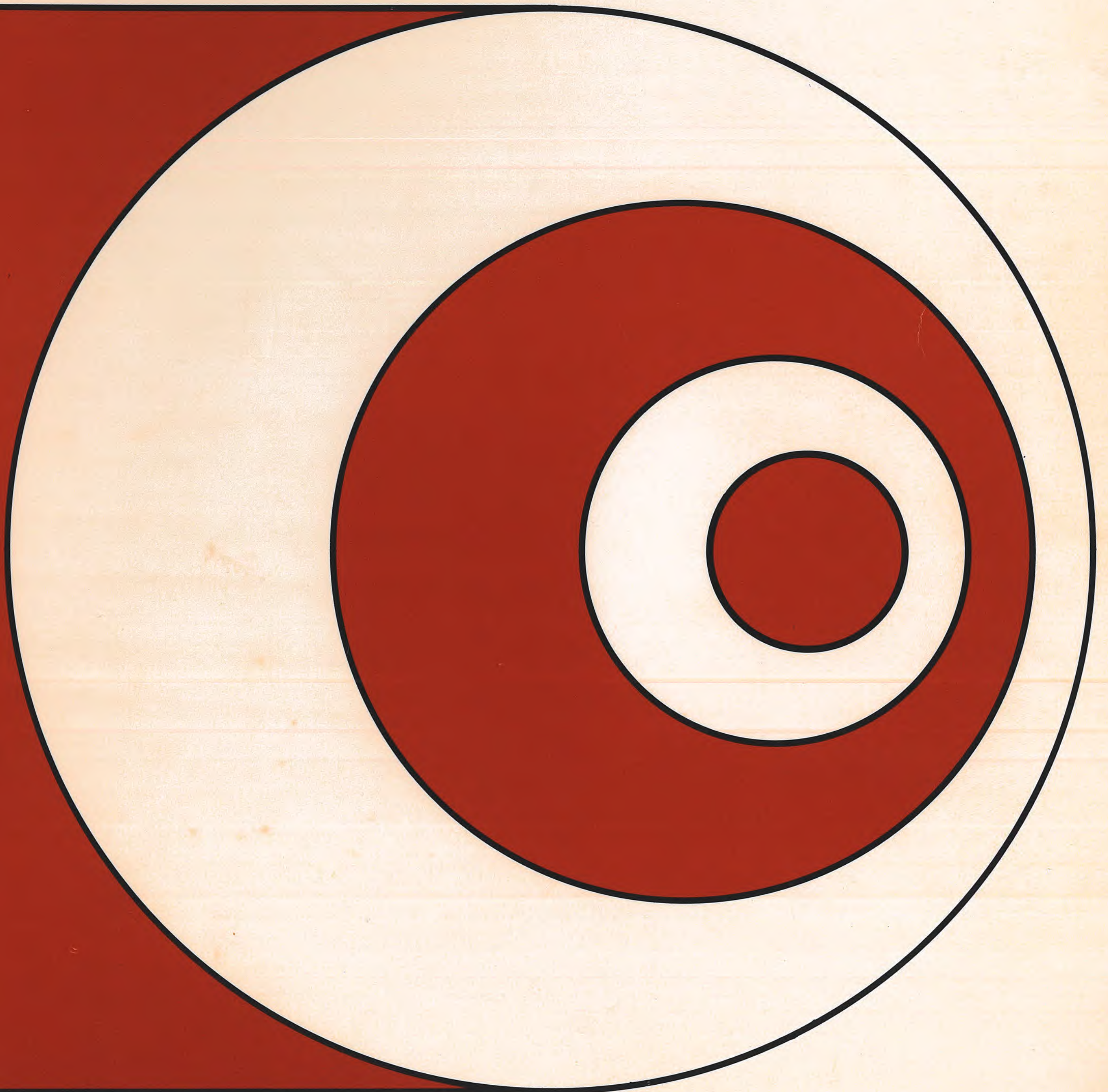
SIGNETICS TWIN
TESTWARE INSTRUMENT

2650 ASSEMBLY LANGUAGE



Signetics TWIN Testware Instrument

2650 ASSEMBLY LANGUAGE MANUAL

signetics

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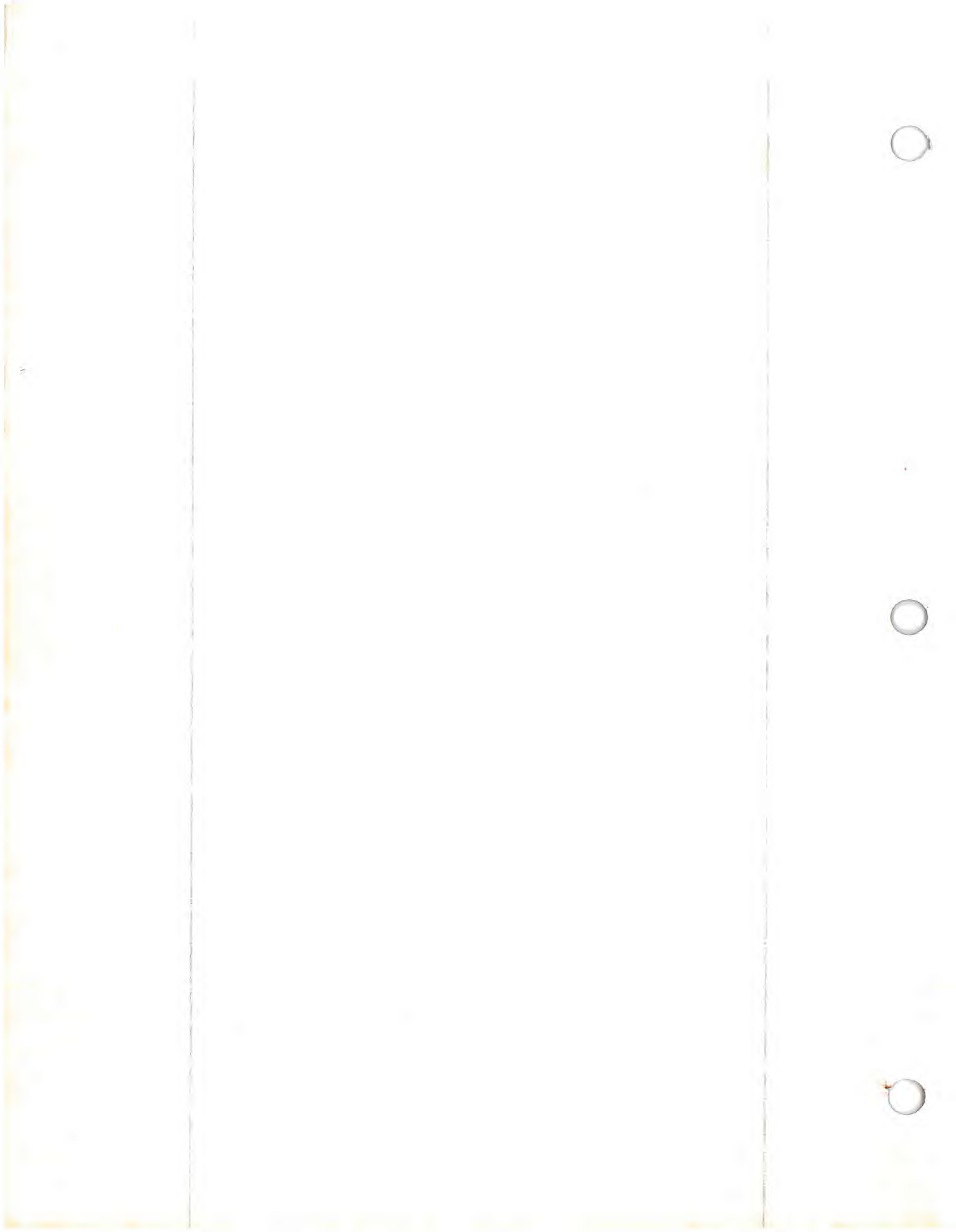

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TWIN 2650
ASSEMBLY LANGUAGE
MANUAL

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I. INTRODUCTION

The 2650 assembly language is a symbolic language designed specifically to facilitate the writing of programs for the Signetics 2650 processor. The 2650 TWIN Assembler is a program which accepts this symbolic source code as input and produces a listing and/or an object module as output.

The 2650 TWIN Assembler runs as an application program in the 2650 Slave CPU of the Signetics TWIN prototype development system. Information regarding operation of the TWIN Assembler is contained in the "TWIN Operator's Guide."

The assembler is a two-pass program that builds a symbol table, issues helpful error messages, produces an easily readable program listing, and outputs a computer readable object (load) module. It features conditional assembly, symbolic and relative addressing, forward references, free format source code, self-defining constants, complex expression evaluation, and a versatile set of Pseudo Operations. Additionally, the assembler is capable of generating data in several number-based systems, including ASCII character code. These features aid the programmer/engineer in producing well documented, working programs in minimum time.

The 2650 TWIN Assembler is upward compatible from the cross-assembler described in the 2650 Microprocessor Manual, except that the TWIN assembler does not recognize the EBCDIC character constant form. However, the TWIN assembler contains several enhancements not present in the cross-assembler. These include conditional assembly, longer labels, and tabbing capability. Information regarding conversion of cross-assembler source programs for use with the TWIN Assembler is contained in Appendix G.

ASSEMBLY LANGUAGE

An **assembly language program** is a program written in **symbolic machine language**. It is comprised of **statements**. A statement is either a **symbolic machine instruction**, a **pseudo-operation** statement, or a **comment**.

A symbolic machine instruction is a written specification for a particular machine operation expressed by a symbolic operation code and, if required, a symbolic address or operand. For example:

```
LOC2        STRR, R0    SAV
```

Where:

LOC2	is a symbol representing the memory address of the instruction.
STRR	is a symbolic operation code representing the bit pattern of the "store relative" instruction.
R0	is a symbol that has been defined as register 0 by the "EQU" pseudo-op.
SAV	is a symbol representing the memory location into which the contents of register 0 are to be stored.

A pseudo-operation statement is a statement which is not translated into a machine instruction, but rather is interpreted as a directive to the assembler program. For example:

SCHD	ACON	REDY

Where:

ACON — is a pseudo-op which directs the assembler program to allocate two bytes of memory.

SCHD — is a symbol. The assembler is to assign the memory address of the first byte of the two allocated to this symbol.

REDY — is a symbol representing an address. The assembler is directed to place the equivalent memory address into the allocated bytes.

STATEMENTS

Statements are always written in a particular format. The format is depicted below:

LABEL FIELD	OPERATION FIELD	OPERAND FIELD	COMMENT FIELD

The statement is always assumed to be written as an 80-column card image.

The **Label Field** is provided to assign symbolic names to bytes of memory. If present, the Label Field must begin in column one.

The **Operation Field** is provided to specify a symbolic operation code or a pseudo-operation code. If present, the Operation Field must either begin past column one or be separated from the Label Field by one or more blanks.

The **Operand Field** is provided to specify arguments for the operation in the Operation Field. The Operand Field, if present, is separated from the Operation Field by one or more blanks.

The **Comment Field** is provided to enable the assembly language programmer to optionally place a message stating the purpose or intent of a statement or a group of statements. The Comment Field must be separated from the preceding field by one or more blanks.

COMMENT STATEMENT

A Comment Statement is a statement that is not processed by the assembler program. It is merely reproduced on the assembly listing. A Comment Statement is indicated by encoding an asterisk in column one. For example:

*THIS IS A COMMENT STATEMENT

Columns 73-80 are never processed by the assembler, but are reproduced on the assembly listing without processing. This field may be used for sequence numbers, if desired.

LOCATION COUNTER

During the assembly process, the assembler maintains a cell that always contains the address of the next memory location to be assembled. This cell is called the Location Counter. It is used by the assembler to assign addresses to assembled bytes, but it is also available to the programmer.

The character "$" is a symbol that the assembler recognizes as the symbolic name of the Location Counter. It may be used like any other symbol, but it may not appear in the label field.

When using the "$," the programmer may think of it as expressing the idea "$" = "address of myself." For example:

108_{16}	BCTR,3	$

The first byte of this branch instruction is in location 108_{16}. The instruction directs the microprocessor to "branch to myself." The Location Counter in this example contains the value 108_{16}.

SYMBOLIC ADDRESSING

As mentioned above, the user can attach a label to an instruction, as shown in the following example:

SAVR	STRR,R0	SAV

The assembler, upon seeing a valid symbol in the label field, assigns the equivalent address (the value of the Location Counter) to the label. In the given example, if the STRR instruction is to be stored in the address H'0127', then the symbol SAVR would be made equivalent to the value H'0127' for the duration of the assembly.

The symbol could then be used anywhere in the source program to refer to the address value or, more typically, it could be used to refer to the instruction location. The important concept is that the address of the instruction need not be known; only the symbol need be used to refer to the instruction location. Thus, when branching to the STRR instruction, one could write:

```
BCTA,3      SAVR
```

When this three-byte branch instruction is translated by the assembler, the address of the STRR instruction is placed in the address field of the branch instruction. Similarly, in the STRR instruction above, the symbol SAV in the Operand Field is replaced by the address of the memory location whose label is SAV.

It is also possible to use symbolic addresses which are near other locations to refer to those locations without defining new labels. For example:

```
        BCTR,3      BEG
        BCTR,0      BEG+4
        ANDZ        3
        BSTR,3      S+48
BEG     LODA,2      PAL
        HALT
        SUBI,2      3
```

In the above example, the instruction "BCTR,3 BEG" refers to the "LODA,2 PAL" instruction. The instruction "BCTR,0 BEG+4" refers to the "SUBI,2 3" instruction.

BEG+4 means the address BEG plus four bytes. This type of expression is called relative symbolic addressing and given a symbolic address; it can be used as a landmark to express several bytes before or after the symbolic address. Examples are:

```
BCTR,3      PAL+23
BSTA,0      STT-18
```

The arguments are evaluated like any other expression and must be in the range -32,768 to +32,767.

II. LANGUAGE ELEMENTS

Input to the assembler consists of a sequence of characters combined to form assembly language elements. These language elements include symbols, instruction mnemonics, constants and expressions which make up the individual program statements that comprise a source program.

CHARACTERS

Alphabetic:	A through Z	
Numeric:	0 through 9	
Special characters:		blank
	(	left parenthesis
	)	right parenthesis
	+	add or positive value
	–	subtract or negative value
	*	asterisk
	'	single quote
	,	comma
	/	slash
	$	dollar sign
	<	less than sign
	>	greater than sign
	#	pound sign
	@	at sign
	?	question mark
	!	exclamation point
	"	double quote
	%	percent sign
		TAB character (ASCII '09')

SYMBOLS

Symbols are formed from combinations of characters. Symbols provide a convenient means of identifying program elements so that they can be referenced by other elements.

1. Symbols may consist of 1 to 6 characters. The first character must be alphabetic. Succeeding characters may be alphabetic, numeric, or the special characters #, @, ?, !, ", and %.

2. Certain symbols are reserved words for the 2650 TWIN assembler and may not be used as statement labels. These symbols are:

   - any mnemonic operation code (see Appendix A).
   - any assembler directive (see Section IV).
   - the symbols ON and OFF.

   Attempted use of these reserved words as valid symbols will result in an error indication on the assembly listing.

3. The character $ is a special symbol which may be used in the argument field of a statement to represent the current value of the Location Counter.

4. The character * is a special symbol which is used as an indirect address indicator.

5. The characters + and – are also used as auto-increment/auto-decrement indicators.

6. The assembler maintains internal tab stops at every eight columns. The Horizontal Tab character (ASCII H'09', CONTROL-I on the TWIN Display Terminal) will cause the listing to be resumed at the next internal tab stop.

The following are examples of valid symbols:

DOP1	RAV3	SEVEN%
AA	TEMZ	AT#12

The following are examples of invalid symbols:

ROUNDOFF	more than six characters
1LAR	begins with a numeric
PA N	imbedded blank
TEN$	unallowed special character
DATA	reserved word

CONSTANTS

A constant is a self-defining language element. Unlike a symbol, the value of a constant is its own "face" value and is invariant. Internal numbers are represented in 2's complement notation. There are two forms in which constants may be written: the Self-Defining Constant and the General Constant.

Self-Defining Constant

The self-defining constant is a form of constant which is written directly in an instruction and defines a decimal value. For example:

```
LODA,R3     BUFF+65
```

In this example, 65 is a self-defining constant. The value of the integer constant expressed by a self-defining constant must be in the range -32,768 to +32,767.

General Constant

The general constant is also written directly in an instruction, but the interpretation of its value is dictated by a code character and delimited by quotation marks.

```
LODA,R3     BUFF+H'3E'
```

In this example, the code letter H specifies that 3E is a hexadecimal constant equivalent to decimal value 62.

The size of a number generated by a general constant form (B, O, D, H) must be in the range -32,768 to +32,767. However, the most important concept to understand when using constant forms is that the final value of a resolved expression must fit the constraints of the actual field destined to contain the value. For example:

```
LODA,R2     PAL+H'3EE2'-H'3EE0'
```

In this case, the argument, when resolved, must fit into the 13 bits in the actual machine instruction. Even though each of the two hexadecimal constants is larger than can fit into 13 bits, the final value of the expression is containable in 13 bits and therefore the constants are permitted. Similarly, the statement DATA H'3FE' is not allowed, as the DATA statement defines one byte quantities and H'3FE' specifies more than 8 bits. Summarily, the size of the evaluated expressions must be less than or equal to their corresponding data fields.

There are 5 types of General Constants usable with the 2650 TWIN Assembler:

Code	Type
B	Binary Constant
O	Octal Constant
D	Decimal Constant
H	Hexadecimal Constant
A	ASCII Character Constant

B: Binary Constant

A binary constant consists of an optionally signed binary number of up to 16 bits enclosed in single quotes and preceded by the letter B, e.g., B'1011011'. Binary information is stored right justified.

O: Octal Constant

An octal constant consists of an optionally signed octal number enclosed by single quotation marks and preceded by the letter O, e.g., O'352'. The value will be right justified.

D: Decimal Constant

A decimal constant consists of an optionally signed decimal number enclosed by single quotation marks and preceded by the letter D, e.g., D'249'. The value will be right justified.

H: Hexadecimal Constant

A hexadecimal constant consists of an optionally signed hexadecimal number enclosed in single quotation marks and preceded by the letter H, e.g., H'3F'. The value will be right justified.

A: ASCII Character Constant

An ASCII character constant consists of a string of ASCII characters enclosed by single quotation marks and preceded by the letter A. For example: A 'HELLO THERE'. Each character will be encoded in 7-bit ASCII and stored in successive bytes. The high-order bit is always set to zero in each allocated byte.

Note: See Appendix G for permissible characters and their equivalent ASCII codes. To specify a single quotation mark as a character constant, it must appear twice in the character string, e.g., A'TYPE''HELP''NOW' will appear in storage as TYPE'HELP'NOW.

MULTIPLE CONSTANT SPECIFICATIONS

General constant forms, when used in DATA and ACON statements, allow multiple specifications within the constant expression. For example: D'52, 21, 208, 27'. A comma separates each byte specification (except in the ASCII form) and successive specifications determine successive bytes of storage. The forms within a single constant expression may be mixed, except that an ASCII form containing more than one character cannot be mixed. Each byte may be optionally signed. For example:

H'Ø3,-F2,+11,-8,33,Ø',O'271,133',255,H'FØ,FF'
O'271,133',A'X',H'Ø,A,B,C'

EXPRESSIONS

An expression is an assembly language element that represents a value. It consists of a single term or a combination of terms separated by arithmetic, logical or relational operators. A term may be a valid symbolic reference, a self-defining constant or a general constant.

The valid operators which may be used in an expression are:

+	for addition (or unary positive sign)
-	for subtraction (or unary negative sign)
*	for multiplication
/	for division
.MOD.	for remainder after division
.NOT.	for one's complement (unary operator)
.AND.	for logical AND
.OR.	for logical OR
.XOR.	for logical EXCLUSIVE OR
.SHR.	for logical shift right
.SHL.	for logical shift left
>	for retrieving the lower byte of a two-byte argument
<	for retrieving the upper byte of a two-byte argument
.EQ.	for equal (=) relation
.NE.	for not equal (≠) relation
.GT.	for greater than (>) relation
.LT.	for less than (<) relation
.GE.	for greater than or equal to (≥) relation
.LE.	for less than or equal to (≤) relation

The relational operators are binary operators which yield a true (H'FF') or false (0) value.

These operators have an implied priority which determines the order in which the operations are performed in multiple operator expressions. The operations specified by the operators of the highest priority are performed first, then those of the second priority, and so forth.

The priority of operators is as follows, with operators on the same line having equal priority:

* / .MOD. .SHR. .SHL.
\+ -
.EQ. .NE. .GT. .LT. .GE. .LE.
.NOT.
.AND.
.OR. .XOR.
< >

Parentheses can be used to override the implied order of operations or to make the expression clearer. For example:

A + B * C	is equivalent to A + (B * C)
.NOT.A-B.MOD.C	is equivalent to .NOT.(A-(B.MOD.C))
A.AND.B-C	is equivalent to A.AND.(B-C)

The expression A.SHR.B shifts the argument A B places towards the right and fills the most-significant bits of A with zeroes. Similarly, A.SHL.B shifts A B places to the left and fills the least-significant bits with zeroes. For example:

H'43'.SHR.1	is equivalent to H'21'
H'21'.SHL.1	is equivalent to H'42'

Examples of valid expressions are:

LOOP	PAL-$
LOOP+5	$-PAL+3
SAM+3-LOOP	BIT-3+H'3B'

Note: The special symbol '$' represents the current value of the Location Counter.

If an expression resolves to a two-byte value where only a single-byte value is required, the assembler will use the least-significant byte as the operand.

SPECIAL OPERATORS

There are two special operators that are recognized by the assembler. They are:

<	less than sign
>	greater than sign

The assembler interprets these operators in a special way:

>	perform a modulo 256 divide (use low-order byte)
<	perform a divide by 256 (use high-order byte)

These special operators are intended to be used to access a two-byte address in one byte parts using a minimum of storage. For example, if it is desired to get the high-order bits of an address (ADDB) into register 2 and the low-order bits into register 1 it could be done as follows:

```
        LODR,R2   APAL
        LODR,R1   APAL+1
        •••
        •••
        •••
APAL    ACON      ADDB
```

or, by utilizing the special operators, it could be done as follows:

```
        LODI,R2   <ADDB
        LODI,R1   >ADDB
```

The first method uses 6 bytes to accomplish what the second method can do in 4 bytes.

The special operators are most often used to facilitate the passing of an address in registers.

III. SYNTAX

Assembly language elements may be combined to symbolically express both 2650 instructions and assembler directives. There are specific rules for writing these instructions. This set of rules is known as the Syntax of the symbolic assembly language.

FIELDS

A statement prepared for processing by the assembler is divided into four fields: the Label Field, the Operation Field, the Operand Field and the Comment Field. Each field is separated by at least one blank character. Only columns 1 through 72 of the card image are scanned by the assembler. Columns 73 through 80 inclusive may be used for any desired purpose.

Label Field

The label field optionally contains a symbolic name which the assembler assigns to the instruction specified in the remaining part of the line. If a name is specified, it must begin in column 1. The assembler assumes that there is no label if column 1 is blank. The label field, if present, must contain only a valid symbol.

Operation Field

The operation field contains a mnemonic code which represents a 2650 processor operation or an assembly directive. The operation field must be present in every non-comment line. See Appendix A for a list of the valid mnemonic codes. Additionally, depending on the instruction type, the operation field may also specify a general purpose register or a condition code.

Operand Field

The operand (or argument) field contains one or more symbols, constants or expressions separated by commas. The argument field specifies storage locations, constants, register specifications and any other information necessary to completely specify a machine operation or an assembler directive. Embedded blanks are not permitted as they are considered field terminators.

Comment Field

The comment field contains any valid characters in any combination. The comment field is not processed by the assembler, but is merely reproduced on the listing next to the accompanying instruction. It is usually used to explain the purpose or intention of a particular instruction or group of instructions.

Comment Line

An entire 72 column line may be utilized to print comments by coding an asterisk (*) in column 1. This entire card is merely reproduced on the assembly listing without processing by the assembler.

SYMBOLS

Symbols are used in the name field of a symbolic machine instruction to identify that particular instruction and to represent its address. Symbols may be used for other purposes, such as the symbolic representation of some memory address, the symbolic representation of a constant, the symbolic representation of a register, etc.

No matter how the symbol is used, it must be defined. A symbol is defined when the assembler knows what value the symbol represents. There is only one way to define a symbol. The symbol must at some time appear either in the label field of an instruction or of an assembler directive. The symbol will be assigned the current value of the Location Counter when it appears in the label field of a machine instruction, or of an ORG, ACON, DATA, or RES pseudo-op. It may be assigned some other value through use of the EQU or SET assembler directives. A symbol may not appear in the name field more than once in a program, because this would cause the assembler to try to redefine an already defined label. The assembler will not do this and will flag all definitions of the particular label as an error. The only exception is that a symbol assigned a value by a SET pseudo-op may have another value assigned by subsequent SET pseudo-ops.

SYMBOLIC REFERENCES

Symbols may be used to refer to storage designations, register assignments, constants, etc. For example:

Address	Label	Operation	Operand
9B	MAZE	DATA	H'F5'
9C		LODA,3	MAZE

The symbolic label "MAZE" represents the address 9B. It is used in the machine instruction at address 9C to tell the assembler to build an instruction LODA,3 9B. The symbolic label, in this case, is a way for the programmer to specify an address without knowing exactly what the address should be when he writes the program. In this example, assume there was a need to modify this sequence of code: a data statement was inserted between the original two statements.

Address	Label	Operation	Operand
99	MAZE	DATA	H'F5'
9A,9B		DATA	H'FE,3A'
9C		LODA,3	MAZE

Even though there was a program change which caused the data at MAZE to be located at address 99, the load instruction referencing the data didn't have to be rewritten because the assembler could provide the proper physical address for the symbolic address MAZE. The instruction at address 9C will be assembled as LODA,3 99.

SYMBOLIC ADDRESSING

When writing instructions in the symbolic assembly language for the 2650, the addresses may be expressed through symbolic equivalents. The assembler will translate the symbolic address to its numeric equivalent during the assembly process.

It is good programming practice to make all address references symbolic, as this greatly eases the programmer's job in producing a working program. To make the register specification symbolic, one could equate a symbol to the register number:

```
RG3      EQU        3
         • • •
         • • •
         • • •
         • • •
         LODA,RG3   MAZE
```

Forward References

A previously defined symbol is one which has appeared in the name field before it is referenced (as above). In contrast, a forward reference is a symbolic reference to a line of code when the symbol has not yet appeared in the name field. For example:

```
         ADDA,2     COEF
         • • •
         • • •
         • • •
COEF     DATA       D'123'
```

Forward references may be used anywhere in a program with the exception of the operand fields of the EQU, SET, RES, IF, and ORG statements.

Relative Addressing

The programmer may reference a memory cell either directly or via relative addressing. To refer directly to a memory cell of symbolic address MAIN, one has merely to use the name MAIN in the argument field of the referencing instruction. For example:

```
BIRA,R2      MAIN
```

It is also possible to express the address of a memory cell symbolically if some nearby cell is symbolically assigned. For example, to load the memory cell which is 5 cells higher in memory than the cell named MAIN, one need only to refer to it as MAIN+5:

```
LODA,2       MAIN+5
```

This latter method is called relative addressing. The relative count must be in the range -32,768 to +32,767.

The Location Counter and Symbol "$"

There is one symbolic name, "$," which is automatically defined by the assembler. This single character name is always symbolically equated to the assembler's Location Counter. Since the Location Counter is used by the assembler during the assembly process and is usually equated to the address of the next byte to be assembled, it represents the address of the instruction or data currently being specified. For example: BCTR,3 $+5. The branch address will be interpreted by the assembler to be the address of the first byte of the branch instruction plus 5 bytes.

Hardware Relative Addressing

When using instructions which use "hardware relative addressing" (as distinguished from relative addressing discussed earlier in this section), it is important to realize the assembler will not only evaluate the expression which is given as an operand address, but will convert it to a hardware relative address (see the Hardware Specifications manual for a description of the addressing modes). For example:

Address	Name	Operation	Argument
100	SAM	LODA,R2	PAL
103		SUBI,R2	-3
105		BIRR,R3	SAM
107	next instruction		

In this code, the BIRR instruction specifies hardware relative addressing. Even though the equivalent value of the symbolic address SAM is 100, the relative addressing instruction requires a displacement relative to the address of the next sequential instruction. Therefore, the operand SAM will be evaluated as = - (current Location Counter+length of BIRR instruction-SAM) = -(105+2-100) = -(+7) = -7. Remember, where the hardware instruction calls for "hardware relative addressing," the expression in the operand field will be evaluated as the displacement from the address of the next sequential instruction. The value of this displacement may range from -64 to +63.

Indirect Addressing

The symbol "*" is used to specify indirect addressing. For example:

```
        BCTA,3      *SAM
        •••
        •••
        •••
SAM     ACON        SUBR
```

In this sequence of instructions, the BCTA instruction specifies indirect addressing. The assembler will set the indirect bit (byte #1, bit #7) to '1' for this instruction.

Auto-Increment and Auto-Decrement

The symbol "+" and "-" are used to specify auto-increment and auto-decrement, respectively. For example:

```
LODA,R0      BUF,R3,+
```

In this instruction, which specifies auto-increment, the assembler sets bits #6 and #5 of byte #1 to "01." This option is specified in the instruction set tables as (,X).

IV. DIRECTIVES TO THE 2650 TWIN ASSEMBLER

There are fifteen directives (pseudo-ops) which the assembler will recognize. These assembler directives, although written much like processor instructions, are simply commands to the assembler instead of to the processor. They direct the assembler to perform specific tasks during the assembly process, but have no meaning to the 2650 processor. These assembler directives are:

ORG
EQU
SET
ACON
DATA
RES
END
EJE
PRT
SPC
TITL
PCH
IF
ELSE
ENDIF

The use of the last three directives listed above (IF, ELSE, and ENDIF) is described in Section V.

ORG — Set Location Counter

The ORG directive sets the assembly Location Counter to the location specified. The assembler assumes an ORG 0 at the beginning of the program if no ORG statement is given.

LABEL	OPERATION	OPERAND
{name}	ORG	expression

Where:

name	optionally provides a symbol whose value will be equated to the value in the Location Counter before the ORG is evaluated.
expression	when evaluated, results in a positive integer value. This value will replace the contents of the location counter, and bytes subsequently assembled will be assigned sequential memory addresses beginning with this value. Any symbols which appear in the argument must have been previously defined.

Examples:

```
LARR    ORG    YORD
STAR    ORG    H'100'
```

EQU Specify a Symbol Equivalence

The EQU directive tells the assembler to equate the symbol in the name field with the evaluatable expression in the operand field. A symbol equivalence defined by an EQU directive cannot be redefined by a subsequent EQU or SET directive and cannot appear in the label field of a statement.

LABEL	OPERATION	OPERAND
name	EQU	expression

Where:

name — is the symbol which is to be assigned some value by the execution of this directive.

expression — is resolved to an integer value. If a symbol is used in the argument, it must have been previously defined.

Examples:

```
PAL     EQU     H'10F'
LOP2    EQU     PAL
RAMP    EQU     SLOP-3+PAL
REG1    EQU     1
```

SET Specify a Symbol Equivalence

The SET directive tells the assembler to equate the symbol in the name field with the expression to be evaluated in the argument field.

The SET directive is identical to the EQU directive, except that the symbol defined by the SET directive may be redefined later in the program by another SET directive.

LABEL	OPERATION	OPERAND
name	SET	expression

ACON Define Address Constant

The ACON directive tells the assembler to allocate two successive bytes of storage. The evaluted argument will be stored in the two bytes, the low-order 8 bits in the second byte and the high-order bits in the first byte. This directive is mainly intended to provide a double byte containing an address for use as the indirect address for any instruction executing in the indirect addressing mode. Any number of operands may be specified with one ACON directive, but the operands may not extend past column 72. Each operand will be allocated two bytes of storage.

LABEL	OPERATION	OPERAND
{ name }	ACON	expression

Where:

name — is an optional label. If specified, the name becomes the symbolic address of the first byte allocated.

expression — is some expression which must resolve to a positive value or zero. If positive, the value should be no larger than that which can be contained in two bytes. Otherwise, only the least-significant bytes are used.

Example:

```
ASUB    ACON    SUBR
        ACON    SUBR,H'AFF0'
```

DATA — Defines Memory Data

The DATA directive tells the assembler to allocate the exact number of bytes required to hold the data specified in the argument field of this directive. Any number of bytes can be specified with one DATA directive, but the argument field may not extend past column 72.

LABEL	OPERATION	OPERAND
{ name }	DATA	expression

Where:

name — is an optional label. If used, the name becomes the symbolic address of the first byte allocated by the directive.

expression — is a general constant, a self-defining constant or a symbolic address. A multiple constant specification in the argument field will cause a corresponding number of bytes to be allocated. Any other expression that can be resolved to a single value will result in one byte being allocated.

Examples:

```
PAL      DATA     LOOP,LOOP+1
         DATA     H'03,22,FC,A1'
         DATA     +127
         DATA     D'28'
DEFINE   DATA     A'THIS IS'
```

Note: If the expression evaluates to a value between 0 and 255, the result is an eight bit absolute binary number. DATA +127 results in H'7F'. Also, if the expression evaluates to a value which is less than 0, the result is a 2's complement, binary number. DATA H'–5' results in H'FB'. If the expression resolves to a value which requires more than one byte, only the least-significant byte is used.

RES — Reserve Memory Storage

The RES directive tells the assembler to reserve contiguous bytes of storage. The number of bytes so reserved is determined by the argument. The reserved bytes are not set to a known value, but rather the effect of this directive is to increment the location counter.

LABEL	OPERATION	OPERAND
{ name }	RES	expression

Where:

name — is an optional label. If used, the name becomes the symbolic address of the first byte allocated.

expression — is some evaluatable expression which must resolve to some positive integer or zero. If a symbol is specified, it must have been previously defined.

Example:

```
LOR      RES      23
MASK     RES      LOR+5
         RES      H'1A'
```

END — End of Assembly

The END directive informs the assembler that the last statement to be assembled has been input and the assembler may proceed with the assembly. The END directive causes the assembler to communicate the program start address to the object module.

LABEL	OPERATION	OPERAND
	END	expression

Where:

expression — is resolved to the starting address of the program. If this parameter is not specified, the start address is set to zero.

EJE — Eject the Listing Page

The EJE directive tells the assembler to advance the listing to the top of the next page regardless of the line position on the current listing page.

The directive is used primarily to organize listing for documentation purposes and does not appear in the listing.

LABEL	OPERATION	OPERAND
	EJE	

PRT — Printer Control

The PRT directive tells the assembler to resume or discontinue printing of the assembled program.

This directive is used primarily to shorten assembly time by listing only that portion of the program which the user needs to see. This directive does not appear in the listing.

LABEL	OPERATION	OPERAND
	PRT	{ON / OFF}

Note: PRT is set ON at the beginning of an assembly.

SPC — Space Control

The SPC directive tells the assembler to skip or space a number of lines.

This directive is used primarily to organize listings for documentation purposes and does not appear in the listing.

LABEL	OPERATION	OPERAND
	SPC	expression

Where:

expression — is some evaluatable expression which must resolve to some positive integer. If the value of this expression is equal to, or greater than, the number of lines remaining on the page, the effect is the same as the EJE directive.

Example:

```
SPC     5
```

TITL Title

The TITL directive tells the assembler to skip to the top of the next page and insert a given title into the main header.

This directive is used primarily for documentation purposes and does not appear in the listing.

LABEL	OPERATION	OPERAND
	TITL	expression

Where:

expression is the title information not to exceed 38 character positions.

Example:

```
        TITL        MAIN PROGRAM
```

PCH Punch Control

The PCH directive tells the assembler to selectively resume or discontinue the output of the load module.

This directive is used primarily to shorten assembly time when a load module is not desired or when only a portion of the load module is desired.

LABEL	OPERATION	OPERAND
	PCH	{ON / OFF}

Note: PCH is set ON at the beginning of an assembly. When PCH OFF is specified, any prior load module data is output.

V. CONDITIONAL ASSEMBLY

The conditional assembly directives allow the programmer to vary the sequence of generated statements. Thus, the programmer can use these instructions to generate different sequences of statements from the same source program.

There are three conditional assembly directives. They are:

IF
ELSE
ENDIF

The format of the IF statement is:

LABEL	OPERATION	OPERAND
{name}	IF	expression

The standard expression rules apply with the addition of the following six relational operators which may be used in relational expressions:

.EQ. .NE. .LT. .GT. .LE. .GE.

The format for relational expressions is

(expression .XX. expression)

where .XX. is any one of the above relational operators.

The format of the ELSE statement is:

LABEL	OPERATION	OPERAND
	ELSE	

The format of the ENDIF statement is:

LABEL	OPERATION	OPERAND
	ENDIF	

Every IF statement must eventually be followed by an ENDIF statement. The use of the ELSE statement is optional, but, if present, it must appear after the IF statement and before the ENDIF statement.

When an IF statement is encountered, the expression or relational expression is evaluated to be either true (not zero) or false (zero). If true, the following source statements are processed until an ENDIF is encountered. However, if an ELSE is encountered during this processing, the statements between the ELSE and the ENDIF are not processed. If false, the source statements following the IF are not processed until an ELSE or ENDIF is encountered, at which time normal processing resumes.

Conditional assembly constructs may be nested but may not be overlapped. Therefore, the end of an inner IF construct (nested) must be encountered before the end of the outer IF construct is encountered.

The assembler listing will contain only those statements actually assembled. The statements between an IF and ENDIF (or ELSE) which do not produce object code do not appear on the listing.

If the optional label is included in the IF statement, the label will be assigned the value of the Location Counter when the next byte is actually assembled.

VI. THE ASSEMBLY PROCESS

The 2650 assembler translates symbolic source code into machine language instructions. The assembler examines every source statement for syntactic validity and produces the equivalent machine code for the 2650 processor.

This is a two pass assembler, which means the entire source code is scanned twice by the assembler. On the first pass, all defined labels and their equivalent values are stored in a symbol table, the first byte of every instruction is fully determined, and some errors may be detected. During pass 2, symbolic address references are replaced by their values, errors may be detected, and a listing and load/object module are generated.

SYMBOL TABLE

The assembler builds and maintains a symbol table during the assembly process. The symbol table contains an entry for each symbol in the assembled program. The entry consists of the symbol itself and its value. If a symbol which appears in the operand field of an instruction has never been defined (never appeared in the label field), the assembler will generate an error code on the listing because it is unable to resolve an undefined symbol and will place zero as the unresolved value in the object module.

LOCATION COUNTER

The assembler maintains a memory cell which it uses as a Location Counter. This Location Counter keeps track of the address of the next byte of storage to be allocated by the assembler. During coding, the programmer may think of the Location Counter as containing the address of the first byte of the instruction being written. In this assembler, the Location Counter is also used to provide load information. This means that the addresses displayed on an assembly listing are the actual addresses which are to contain the corresponding information upon loading of the object program.

ERROR DETECTION

During an assembly, the source program is checked for syntax errors. If errors are found, appropriate notification is given and the assembly proceeds. Although an assembled program containing errors generally will not run properly, it is considered good practice to complete the assembly to locate all errors at one time, rather than terminate it when an error is encountered.

ERROR CODES

There is a column on the listing in which an error indication may appear. Sometimes, because an error causes the assembler to view a subsequent statement incorrectly, a valid statement may be flagged as an error. A good rule is to fix errors in a particular line of code as they are discovered.

The following alphabetic characters are printed in the error indicator column and imply the corresponding message.

L— Label error. The label contains too many characters, contains invalid characters, has been previously defined, or is an invalid symbol.

O— Op-code error. The op-code mnemonic has not been recognized as a valid mnemonic.

R— Register field error. The register field expression could not be evaluated, or when evaluated, was less than 0 or greater than 3, or the register field was not found.

S— Syntax error. The instruction has violated some syntax rule.

U— Undefined symbol. There is a symbol in the argument field which has not been previously defined.

A— Argument error. The argument has been coded in such a way that it cannot be resolved to a unique value.

P— Paging error. A memory access instruction has attempted to address across a page boundary.

W—Warning. The assembler has detected a syntactically correct but unusual construction. The error will be counted but will not inhibit the production of the object module.

If more than one error occurs in a single statement, only the indicator for the first error encountered will be printed.

ASSEMBLY LISTING

Figure VI-I is a sample of a program listing produced by the 2650 TWIN Assembler. The following explanations are keyed to the listing.

1. Page heading — displays the current version and level of the 2650 TWIN Assembler and the title, if any, specified by the TITL assembler directive.
2. Page number — Every page of the listing is numbered sequentially.
3. Line number — This number corresponds to the line number of the source program file.
4. Address column — The numbers in this column are equal to the value of the assembly Location Counter and indicate the address at which the first byte is located. For the EQU and SET directives, this column contains the hexadecimal value of the expression field.
5. Object — This field describes the data bytes which are stored sequentially starting at the address in the Address Column.
6. Error column — This column may contain an error code as detailed elsewhere in this chapter.
7. Source code — This area of the listing reproduces the source code as it was read by the assembler.
8. Total errors — This field indicates the total number of errors detected by the assembler during the assembly process.

Figure VI-I

```
TWIN ASSEMBLER VER 1.0     SAMPLE PROGRAM LISTING                PAGE 0001

LINE ADDR  OBJECT E SOURCE

0002                  * ARITHMETIC BUBBLE SORT PROGRAM
0003 0000             R0   EQU      0
0004 0001             R1   EQU      1
0005 0002             R2   EQU      2
0006 0003             R3   EQU      3
0007 0003             UN   EQU      3
0008 0001             GT   EQU      1
0009 0002             LT   EQU      2
0010 0000             EQ   EQU      0
0011 0000 00          ZERO DATA     0
0012 0001             CNT  RES      1           NUMBER OF ITERATIONS
0013                  *
0014                  *
0015                  * MAIN PROGRAM
0016 0002 0F00C8      STRT LODA,R3  LEN         LOAD BUF LENGTH IN R3
0017 0005 7502             CPSL     2           SET FOR ARITH COMPARISONS
0018 0007 A701        SORT SUBI,R3  1           DECREMENT LOOP COUNTER
0019 0009 CF0001           STRA,R3  CNT         STORE LOOP COUNTER
0020 000C 7F0012           BSNA,R3  SUB1        IF NOT 0, CALL SUBROUTINE
0021 000F 5B76             BRNR,R3  SORT        IF NOT 0, LOOP BACK AGAIN
0022 0011 40               HALT
0023                  *
0024                  * SUBROUTINE FOR ONE ITERATION THROUGH BUFFER
0025 0012 0E0000      SUB1 LODA,R2  ZERO        R2 COUNTS COMPARISONS
0026 0015 EE0001      LOOP COMA,R2  CNT         IF =, ITERATION COMPLETE
0027 0018 14               RETC,EQ
0028 0019 0E60C9           LODA,R0  BUF,R2      LOAD FIRST # OF THE PAIR
0029 001C EE20C9           COMA,R0  BUF,R2,+    COMPARE WITH SECOND #
0030 001F 9974             BCFR,GT  LOOP        IF FIRST LT OR =,LOOP BACK
0031 0021 C1               STRZ     R1          MOVE LARGER # TO R1
0032 0022 0E60C9           LODA,R0  BUF,R2      LOAD SMALLER # INTO R0
0033 0025 CE60C8           STRA,R0  BUF-1,R2    STORE SMALLER # FIRST
0034 0028 01               LODZ     R1          MOVE LARGER # TO R0
0035 0029 CE60C9           STRA,R0  BUF,R2      STORE LARGER # SECOND
0036 002C 1B67             BCTR,UN  LOOP        LOOP BACK
0037                  *
0038                  *
0039 002E                  ORG      200
0040 00C8 0F          LEN  DATA     15          LENGTH OF BUFFER
0041 00C9             BUF  RES      15          BUFFER TO BE SORTED
0042 0002                  END      STRT

 TOTAL ASSEMBLY ERRORS = 0000
```

APPENDIX A
SUMMARY OF 2650 INSTRUCTION MNEMONICS

In these tables parentheses are used to indicate options. In no case are they coded in any instruction. The following abbreviations are used:

r — register expression, must evaluate to $0 \leqslant r \leqslant 3$.
v — value expression
* — indirect indicator
a — address expression
x — index register expression
X — index register expression with optional auto-increment or auto-decrement

Note

— The use of the indirect indicator is always optional.

— When an index register expression is specified, it can be followed by ',+' or ',—' which indicates use of auto-increment or auto-decrement of the index register. Example:

LODA,0 DPR,R3,+

BXA, BSXA are exceptions and do not permit auto-increment or auto-decrement.

— Even though an address expression is specified in a hardware relative addressing instruction, the assembler develops it into a value of $(-64 \leqslant v \leqslant +63)$.

— A memory reference instruction which requires indexing may use only register 0 as the destination of the operation.

— If an index register expression is used with either BXA or BSXA instructions, it must specify index register #3 (either register bank) for indexing. Any other value in the index field will produce an error during assembly. However, it is not necessary to use an index register expression with these instructions: a blank in this field will default to register 3.

LOAD/STORE INSTRUCTIONS

			Length (bytes)
LODZ	r	Load Register Zero	1
LODI,r	v	Load Immediate	2
LODR,r	(*)a	Load Relative	2
LODA,r	(*)a(,X)	Load Absolute	3
STRZ	r	Store Register Zero	1
STRR,r	(*)a	Store Relative	2
STRA,r	(*)a(,X)	Store Absolute	3

ARITHMETIC INSTRUCTIONS

ADDZ	r	Add to Register Zero	1
ADDI,r	v	Add Immediate	2
ADDR,r	(*)a	Add Relative	2
ADDA,r	(*)a(,X)	Add Absolute	3
SUBZ	r	Subtract from Register Zero	1
SUBI,r	v	Subtract Immediate	2
SUBR,r	(*)a	Subtract Relative	2
SUBA,r	(*)a(,X)	Subtract Absolute	3

LOGICAL INSTRUCTIONS

ANDZ	r	And to Register Zero	1
ANDI,r	v	And Immediate	2
ANDR,r	(*)a	And Relative	2
ANDA,r	(*)a(,X)	And Absolute	3
IORZ	r	Inclusive or to Register Zero	1
IORI,r	v	Inclusive or Immediate	2
IORR,r	(*)a	Inclusive or Relative	2
IORA,r	(*)a(,X)	Inclusive or Absolute	3
EORZ	r	Exclusive or to Register Zero	1
EORI,r	v	Exclusive or Immediate	2
EORR,r	(*)a	Exclusive or Relative	2
EORA,r	(*)a(,X)	Exclusive or Absolute	3

COMPARISON INSTRUCTIONS

COMZ	r	Compare to Register Zero	1
COMI,r	v	Compare Immediate	2
COMR,r	(*)a	Compare Relative	2
COMA,r	(*)a(,X)	Compare Absolute	3

ROTATE INSTRUCTIONS

RRR,r		Rotate Register Right	1
RRL,r		Rotate Register Left	1

BRANCH INSTRUCTIONS

BCTR,v	(*)a	Branch on Condition True Relative	2
BCFR,v	(*)a	Branch on Condition False Relative	2
BCTA,v	(*)a	Branch on Condition True Absolute	3
BCFA,v	(*)a	Branch on Condition False Absolute	3
BRNR,r	(*)a	Branch on Register Non-Zero Relative	2
BRNA,r	(*)a	Branch on Register Non-Zero Absolute	3
BIRR,r	(*)a	Branch on Incrementing Register Relative	2
BIRA,r	(*)a	Branch on Incrementing Register Absolute	3
BDRR,r	(*)a	Branch on Decrementing Register Relative	2
BDRA,r	(*)a	Branch on Decrementing Register Absolute	3
BXA	(*)a(,x)	Branch Indexed Absolute, Unconditional	3
ZBRR	(*)a	Zero Branch Relative, Unconditional	2

SUBROUTINE BRANCH/RETURN INSTRUCTIONS

			Length (bytes)
BSTR,v	(*)a	Branch to Subroutine on Condition True, Relative	2
BSFR,v	(*)a	Branch to Subroutine on Condition False, Relative	2
BSTA,v	(*)a	Branch to Subroutine on Condition True, Absolute	3
BSFA,v	(*)a	Branch to Subroutine on Condition False, Absolute	3
BSNR,r	(*)a	Branch to Subroutine on Non-Zero Register, Relative	2
BSNA,r	(*)a	Branch to Subroutine on Non-Zero Register, Absolute	3
BSXA	(*)a(,x)	Branch to Subroutine, Indexed, Unconditional	3
RETC,v		Return From Subroutine, Conditional	1
RETE,v		Return From Subroutine and Enable Interrupt, Conditional	1
ZBSR	(*),a	Zero Branch to Subroutine Relative, Unconditional	2

PROGRAM STATUS INSTRUCTIONS

LPSU		Load Program Status, Upper	1
LPSL		Load Program Status, Lower	1
SPSU		Store Program Status, Upper	1
SPSL		Store Program Status, Lower	1
CPSU	v	Clear Program Status, Upper, Selective	2
CPSL	v	Clear Program Status, Lower, Selective	2
PPSU	v	Preset Program Status, Upper, Selective	2
PPSL	v	Preset Program Status, Lower, Selective	2
TPSU	v	Test Program Status, Upper, Selective	2
TPSL	v	Test Program Status Lower, Selective	2

INPUT/OUTPUT INSTRUCTIONS

WRTD,r		Write Data	1
REDD,r		Read Data	1
WRTC,r		Write Control	1
REDC,r		Read Control	1
WRTE,r	v	Write Extended	2
REDE,r	v	Read Extended	2

MISCELLANEOUS INSTRUCTIONS

HALT		Halt, Enter Wait State	1
DAR,r		Decimal Adjust Register	1
TMI,r	v	Test Under Mask Immediate	2
NOP		No Operation	1

APPENDIX B
NOTES ABOUT THE 2650 MICROPROCESSOR

1. AUTO-INCREMENT, DECREMENT of index register. This feature is optional on any instruction which used indexing with the exception of BXA and BSXA. The increment or decrement occurs before the index register is added to the displacement in the instruction.

2. The contents of registers when used for indexing are considered to be unsigned absolute numbers. Consequently, index registers can contain values from 0 to 255. They "wrap-around" so that the number following 255 is 0.

3. Only absolute addressing instructions can be indexed.

4. The Branch on Incrementing Register or Decrementing Register instructions perform the increment or decrement before testing for zero. The only time the branch is not made is when the register contains zero.

5. All hardware relative addressing is implemented as modulo 8K and therefore relative addressing across the top of a page boundary will result in a physical address near the bottom of the page being accessed. For example:

   $1FFC_{16}$ LODR,R2 $+16

   This instruction results, during execution, in accessing the byte at location 000C in the same page as the instruction. Similarly, negative relative addresses from near the bottom of a page may result in an effective address near the top of the page.

6. Page boundaries cannot be indexed across.

7. Data can always be accessed across a page boundary through use of relative indirect or absolute indirect addressing modes.

8. The only way to transfer control to a program in some other page is to branch absolute or branch indirectly to the new page. Program execution cannot flow across a page boundary.

9. Unconditional branch or branch to subroutine instructions are coded by specifying a value of 3 in the register/value field of BSTA, BSTR, BCTA or BCTR. Example:

```
UN      EQU       3
        •••
        •••
        •••
        BSTA,UN   PAL
        BCTR,3    LOOP
```

   Unconditional branches or subroutine branches on condition false (BCFA, BCFR, BSFA, BSFR) are not allowed.

APPENDIX C
ASCII CODE

This table presents the only characters that the assembler will recognize in an A type constant and their equivalent codes in hexadecimal.

<table>
<tr><th>VALID CHARACTERS</th><th>ASCII CODE</th><th>VALID CHARACTERS</th><th>ACSII CODE</th></tr>
<tr><td>0</td><td>30</td><td>V</td><td>56</td></tr>
<tr><td>1</td><td>31</td><td>W</td><td>57</td></tr>
<tr><td>2</td><td>32</td><td>X</td><td>58</td></tr>
<tr><td>3</td><td>33</td><td>Y</td><td>59</td></tr>
<tr><td>4</td><td>34</td><td>Z</td><td>5A</td></tr>
<tr><td>5</td><td>35</td><td>blank</td><td>20</td></tr>
<tr><td>6</td><td>36</td><td>.</td><td>2E</td></tr>
<tr><td>7</td><td>37</td><td>(</td><td>28</td></tr>
<tr><td>8</td><td>38</td><td>+</td><td>2B</td></tr>
<tr><td>9</td><td>39</td><td>|</td><td>7C</td></tr>
<tr><td>A</td><td>41</td><td>&</td><td>26</td></tr>
<tr><td>B</td><td>42</td><td>!</td><td>21</td></tr>
<tr><td>C</td><td>43</td><td>$</td><td>24</td></tr>
<tr><td>D</td><td>44</td><td>*</td><td>2A</td></tr>
<tr><td>E</td><td>45</td><td>)</td><td>29</td></tr>
<tr><td>F</td><td>46</td><td>;</td><td>3B</td></tr>
<tr><td>G</td><td>47</td><td>¬ or ~</td><td>7E*</td></tr>
<tr><td>H</td><td>48</td><td>–</td><td>2D</td></tr>
<tr><td>I</td><td>49</td><td>/</td><td>2F</td></tr>
<tr><td>J</td><td>4A</td><td>,</td><td>2C</td></tr>
<tr><td>K</td><td>4B</td><td>%</td><td>25</td></tr>
<tr><td>L</td><td>4C</td><td>– or ←</td><td>5F*</td></tr>
<tr><td>M</td><td>4D</td><td>></td><td>3E</td></tr>
<tr><td>N</td><td>4E</td><td>?</td><td>3F</td></tr>
<tr><td>O</td><td>4F</td><td>:</td><td>3A</td></tr>
<tr><td>P</td><td>50</td><td>#</td><td>23</td></tr>
<tr><td>Q</td><td>51</td><td>@</td><td>40</td></tr>
<tr><td>R</td><td>52</td><td>'</td><td>27</td></tr>
<tr><td>S</td><td>53</td><td>=</td><td>3D</td></tr>
<tr><td>T</td><td>54</td><td>"</td><td>22</td></tr>
<tr><td>U</td><td>55</td><td><</td><td>3C</td></tr>
</table>

*may have different graphic symbols on different output devices.

APPENDIX D

ASCII CHARACTER SET

ACSII CHARACTER SET (7-BIT CODE)									
L.S. CHAR \ M.S. CHAR		0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	NUL	DLE	SP	0	@	P	`	p
1	0001	SOH	DC1	!	1	A	Q	a	q
2	0010	STX	DC2	"	2	B	R	b	r
3	0011	ETX	DC3	#	3	C	S	c	s
4	0100	EOT	DC4	$	4	D	T	d	t
5	0101	ENQ	NAK	%	5	E	U	e	u
6	0110	ACK	SYN	&	6	F	V	f	v
7	0111	BEL	ETB	'	7	G	W	g	w
8	1000	BS	CAN	(	8	H	X	h	x
9	1001	HT	EM	)	9	I	Y	i	y
A	1010	LF	SUB	*	:	J	Z	j	z
B	1011	VT	ESC	+	;	K	[	k	{
C	1100	FF	FS	,	<	L	\	l	|
D	1101	CR	GS	–	=	M	]	m	}
E	1110	SO	RS	•	>	N	↑	n	~
F	1111	SI	US	/	?	O	← or _	o	DEL

APPENDIX E
POWERS OF TWO TABLE

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 45
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5

APPENDIX F
HEXADECIMAL-DECIMAL CONVERSION TABLES

From hex: locate each hex digit in its corresponding column position and note the decimal equivalents. Add these to obtain the decimal value.

From decimal: (1) locate the largest decimal value in the table that will fit into the decimal number to be converted, and (2) note its hex equivalent and hex column position. (3) Find the decimal remainder. Repeat the process on this and subsequent remainders.

The table on pages 32-35 provides for direct conversion of hexadecimal and decimal numbers in these ranges:

Hexadecimal	Decimal
000 to FFF	0000 to 4095

In the table, the decimal value appears at the intersection of the row representing the most significant hexadecimal digits (16^2 and 16^1) and the column representing the least significant hexadecimal digit (16^0).

Example: $C21_{16} = 3105_{10}$

HEX	0	1	2
C0	3072	3073	3074
C1	3088	3089	3090
C2	3104	3105	3106
C3	3120	3121	3122

HEXADECIMAL COLUMNS											
6		5		4		3		2		1	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
BYTE 1				BYTE 2				BYTE 3			

Appendix F (Continued)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
01	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
02	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
03	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
04	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
05	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
06	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
07	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
08	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
09	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
10	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
11	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
12	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
13	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
14	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
15	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
16	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
17	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
18	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
19	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
20	0512	0513	0514	0515	0516	0517	0518	0519	0520	0521	0522	0523	0524	0525	0526	0527
21	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
22	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
23	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
24	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
25	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
26	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
27	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
28	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
29	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
30	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
31	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
32	0800	0801	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
33	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
34	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
35	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
36	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
37	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895
38	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
39	0912	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

Appendix F (Continued)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
40	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
41	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
42	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
43	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
44	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
45	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
46	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
47	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
48	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
49	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
50	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
51	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
52	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
53	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
54	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
55	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
56	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
57	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
58	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
59	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
60	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
61	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
62	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
63	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
64	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
65	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
66	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
67	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
68	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
69	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
6C	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
70	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
71	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
72	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
73	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
74	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
75	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
76	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
77	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
78	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
79	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047

Appendix F (Continued)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
80	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
81	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
82	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
83	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
84	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
85	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
86	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
87	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
88	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
89	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
90	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
91	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
92	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
93	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
94	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
95	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399
96	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415
97	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
98	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
99	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A	2464	2465	2466	2467	2468	2469	2470	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
A0	2560	2561	2562	2563	2564	2565	2566	2567	2568	2569	2570	2571	2572	2573	2574	2575
A1	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A2	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A3	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618	2619	2620	2621	2622	2623
A4	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A5	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A6	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A7	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A8	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A9	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC0	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD0	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE0	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF0	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
B0	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B1	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B2	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B3	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B4	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B5	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B6	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B7	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B8	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B9	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071

Appendix F (Continued)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C0	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C1	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C2	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C3	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C4	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C5	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C6	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C7	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C8	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C9	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
D0	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D1	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D2	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D3	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D4	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D5	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D6	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D7	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D8	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D9	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E0	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E1	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E2	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E3	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E4	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E5	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E6	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E7	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E8	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E9	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F0	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F1	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F2	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F3	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F4	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F5	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F6	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F7	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F8	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F9	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

APPENDIX G
CONVERSION OF CROSS-ASSEMBLER SOURCE PROGRAMS

Signetics' 2650 Assembly Language programs, originally written to be assembled with the 16-bit, 32-bit, or GE or NCSS timesharing cross-assembler, may require minor modification in order to produce an error-free assembly on the TWIN resident assembler. The following items should be noted with regard to the TWIN assembler:

1. All instruction mnemonics (Appendix A), all assembler directive pseudo-ops (Section IV), and the words ON and OFF are reserved words and may not be used for symbols.

2. The EBCDIC character form (e.g., E'HELLO') is not valid.

3. The characters '—' and '/' embedded in an expression will be interpreted as multiplication and division operators, respectively.

4. The range of numbers handled by the TWIN assembler is -32,768 to +65,535. If the intermediate value of an expression exceeds this range, an unflagged error in the object code may result.

5. The operand field in the TITL assembler directive is limited to 38 characters.

6. The END assembler directive requires an expression. This expression should resolve to the starting address value.

APPENDIX H
TWIN ASSEMBLER GRAMMAR

The TWIN Assembler grammar is presented below in the Backus notation, where the language is given as a set of syntax equations. Each syntax equation defines a particular language element, called a non-terminal symbol, enclosed within brackets on the left of the equation. The defined symbol is separated from its definition by the symbol "::=" and alternative definitions are separated by the "|" symbol. Symbols occurring in the language are not enclosed within broken brackets, and are not called terminal symbols. Certain non-terminal symbols, however, are not further defined, since they are completely described in earlier sections of this manual. These non-terminals are:

⟨identifier⟩	a valid symbol
⟨number⟩	an integer constant with binary, octal, decimal, or hexadecimal radix
⟨string⟩	an ASCII string of one or two characters
⟨chr-string⟩	an ASCII string of more than two characters
⟨blk⟩	one or more spaces

Note that an ⟨expression⟩ occurs in the grammar in nearly all language constructions where a literal or address constant would be expected. In these cases, the assembler checks to ensure that the ⟨expression⟩ does, in fact, resolve to a literal or address constant according to the restrictions given in previous sections of this manual where the construct is presented.

The following is the input grammar:

```
⟨PROGRAM LINE⟩::= ⟨IDENTIFIER⟩ ⟨BLK⟩ ⟨STATEMENT⟩
               | ⟨BLK⟩ ⟨STATEMENT⟩

⟨STATEMENT⟩    ::= ⟨OPCOD1⟩
               | ⟨OPCODA⟩, ⟨REG⟩
               | ⟨OPCOD2⟩ ⟨BLK⟩ ⟨REG⟩
               | ⟨OPCOD3⟩ ⟨BLK⟩ ⟨VALUE⟩
               | ⟨OPCOD4⟩, ⟨REG⟩ ⟨BLK⟩ ⟨VALUE⟩
               | ⟨OPCOD5⟩, ⟨REG⟩ ⟨BLK⟩ ⟨ADDR-FORM1⟩
               | ⟨OPCOD6⟩, ⟨REG⟩ ⟨BLK⟩ ⟨ADDR-FORM2⟩
               | ⟨OPCOD7⟩, ⟨VALUE⟩ ⟨BLK⟩ ⟨ADDR-FORM1⟩
               | ⟨OPCOD8⟩ ⟨BLK⟩ ⟨ADDR-FORM1⟩
               | ⟨OPCOD9⟩ ⟨BLK⟩ ⟨ADDR-FORM2⟩
               | ⟨PSOP1⟩
               | ⟨PSOP2⟩ ⟨BLK⟩ ⟨ADDRESS⟩
               | ⟨PSOP3⟩ ⟨BLK⟩ ⟨EXPRESSION⟩
               | ⟨PSOP4⟩ ⟨BLK⟩ ⟨CHR-STRING⟩
               | ⟨PSOP4⟩ ⟨BLK⟩ ⟨EXPR-STR⟩
               | ⟨PSOP5⟩ ⟨BLK⟩ ⟨ON-OFF⟩
               | IF ⟨BLK⟩ ⟨EXPRESSION⟩

⟨REG⟩          ::= ⟨EXPRESSION⟩

⟨VALUE⟩        ::= ⟨EXPRESSION⟩

⟨ADDR-FORM1⟩   ::= ⟨ADDRESS⟩
               | * ⟨ADDRESS⟩

⟨ADDR-FORM2⟩   ::= ⟨ADDR-FORM1⟩
               | ⟨ADDR-FORM1⟩, ⟨REG⟩
               | ⟨ADDR-FORM1⟩, ⟨REG⟩, +
               | ⟨ADDR-FORM1⟩, ⟨REG⟩, –

⟨ADDRESS⟩      ::= ⟨EXPRESSION⟩

⟨EXPRESSION⟩   ::= ⟨LOG-EXP⟩
               | < ⟨LOG-EXP⟩
               | > ⟨LOG-EXP⟩

⟨LOG-EXP⟩      ::= ⟨LOG-EXP⟩ .OR. ⟨LOG-PRI⟩
               | ⟨LOG-EXP⟩ .XOR. ⟨LOG-PRI⟩
               | ⟨LOG-PRI⟩

⟨LOG-PRI⟩      ::= ⟨LOG-SEC⟩
               | ⟨LOG-PRI⟩ .AND. ⟨LOG-SEC⟩

⟨LOG-SEC⟩      ::= .NOT. ⟨REL-EXPRESSION⟩
               | ⟨REL-EXPRESSION⟩

⟨ARITH-EXP⟩    ::= ⟨ARITH-EXP⟩ + ⟨TERM⟩
               | ⟨ARITH-EXP⟩ – ⟨TERM⟩
               | ⟨TERM⟩
               | – ⟨TERM⟩
               | + ⟨TERM⟩

⟨TERM⟩         ::= ⟨PRI⟩
               | ⟨TERM⟩ * ⟨PRI⟩
               | ⟨TERM⟩ / ⟨PRI⟩
               | ⟨TERM⟩ .MOD. ⟨PRI⟩
               | ⟨TERM⟩ .SHR. ⟨PRI⟩
               | ⟨TERM⟩ .SHL. ⟨PRI⟩

⟨PRI⟩          ::= ( ⟨EXPRESSION⟩ )
               | ⟨NUMBER⟩
               | ⟨IDENTIFIER⟩
               | ⟨STRING⟩
               | $

⟨REL-EXPRESSION⟩ ::= ⟨ARITH-EXP⟩
               | ⟨REL-EXPRESSION⟩ ⟨IF-REL⟩
                   ⟨ARITH-EXP⟩

⟨EXPR-STR⟩     ::= ⟨EXPR-STR⟩, ⟨EXPRESSION⟩
               | ⟨EXPRESSION⟩
```

```
<OPCODA>      ::= DAR
               | RRR
               | RRL
               | WRTD
               | REDD
               | WRTC
               | REDC
               | RETC
               | RETE

<OPCOD1>      ::= HALT
               | NOP
               | LPSU
               | LPSL
               | SPSU
               | SPSL

<OPCOD2>      ::= LODZ
               | STRZ
               | ADDZ
               | SUBZ
               | ANDZ
               | IORZ
               | EORZ
               | COMZ

<OPCOD3>      ::= CPSU
               | CPSL
               | PPSU
               | PPSL
               | TPSU
               | TPSL

<OPCOD4>      ::= LODI
               | ADDI
               | SUBI
               | ANDI
               | IORI
               | EORI
               | COMI
               | TIMI
               | WRTE
               | REDE

<OPCOD5>      ::= LODR
               | STRR
               | ADDR
               | SUBR
               | ANDR
               | IORR
               | EORR
               | COMR
               | BRNR
               | BIRR
               | BIRA
               | BDRR
               | BDRA
               | BSNR
               | BSNA

<OPCOD6>      ::= LODA
               | STRA
               | ADDA
               | SUBA
               | ANDA
               | IORA
               | EORA
               | COMA

<OPCOD7>      ::= BCTR
               | BCTA
               | BCFA
               | BSTR
               | BSFR
               | BSTA
               | BSFA

<OPCOD8>      ::= ZBRR
               | ZBSR

<OPCOD9>      ::= BXA
               | BSXA

<PSOP1>       ::= EJE
               | ELSE
               | ENDIF
               | TITL

<PSOP2>       ::= END
               | ORG

<PSOP3>       ::= EQU
               | RES
               | SET
               | SPC

<PSOP4>       ::= ACON
               | DATA

<PSOP5>       ::= PRT
               | PCH

<IF-REL>      ::= .EQ.
               | .GE.
               | .GT.
               | .LE.
               | .LT.
               | .NE.
```

NOTES

NOTES

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